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APPLICATION

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TITLE: **NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC**

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NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC

BACKGROUND

In digital signaling, the voltage swing of the signal often encounters significant noise. This is especially the case with low voltage signals at a high speed interface. In such applications, problems such as power noise or ground noise can be the result of simultaneous switching of input/output (I/O) buffers, signal reflections, or signal cross-talk. Noise can also result from a weakened physical interconnection caused by a bad solder joint, an improper connection, etc. The result of such noise is the reduction of signal voltage margin as well as degradation of signal performance and reliability.

Figure 1A shows a graphical depiction of an example of an ideal signal 10. The graph represents the voltage of the signal as depicted over time. VREF represents the mid-point reference of the voltage. VREF_L represents the lower voltage boundary. Any signal voltage level below this point, is considered a LOW signal value. VREF_H represents the high voltage boundary. Any signal voltage level above this point is considered a HIGH signal value.

In Figure 1A, the signal 10 starts LOW and transitions to HIGH before returning to LOW. The signal 10 clearly and unambiguously makes the successful transition in signal value. However, Figure 1B shows the effect on the signal 20 of noise caused by a ground glitch. The signal 20 never clearly makes the transition from LOW to HIGH. Instead, it is stuck in the transitional area between VREF_L and VREF_H. Figure 1C shows the effect on the signal 30 of noise caused by a power glitch. The signal 30 never clearly makes the transition from HIGH to LOW. As with the ground glitch of Figure 1B, the signal is stuck in the same transitional area without a clear, discernable value. Finally, Figure 1D

shows an example of the effect of a high resistance path. The signal 40 never crosses VREF_L during its transition from HIGH to LOW. As seen in the previous examples, its value it indeterminate.

In general, electrical characterization of noise related problems require proper software support in generating data patterns and robust hardware support to determine the transient voltage. A common method of debugging a system involves pin by pin testing to find signal voltage errors. This is a very costly and time-consuming operation whether in the laboratory, in the production facility, or in the field.

SUMMARY OF INVENTION

In some aspects the invention relates to an apparatus for detecting a noise error of a signal comprising: a high comparator that references a high voltage limit with the signal and generates an output; a low comparator that references a low voltage limit with the signal and generates an output; and a circuit that processes the high comparator output and the low comparator output, wherein the circuit generates an alarm if a noise error is detected.

In an alternative embodiment, the invention relates to an apparatus for detecting a noise error of a signal comprising: means for detecting a high voltage noise error; means for detecting a low voltage noise error; and means for activating an alarm signal upon detection of the high voltage or the low voltage noise error.

In an alternative embodiment, the invention relates to a method for detecting a noise error of a signal comprising: comparing a high signal voltage with a high reference voltage; activating an alarm if the high signal voltage is less

than the high reference voltage; comparing a low signal voltage with a low reference voltage; and activating an alarm if the low signal voltage is greater than the low reference voltage.

The advantages of the invention include, at least, the ability of a digital circuit to perform a self-diagnosis of signal noise error without pin-by-pin or other time intensive debugging methods. Another advantage of the disclosed invention includes the ability for the circuit to perform self-diagnosis of signal noise error in the test lab, at production quality control, or during actual usage.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1A shows a graph of an ideal signal voltage.

Figure 1B shows a graph of a signal voltage affected by ground glitch noise.

Figure 1C shows a graph of a signal voltage affected by power glitch noise.

Figure 1D shows a graph of a signal voltage affected by high resistance of the signal path.

Figure 2 shows a schematic of one embodiment of a noise margin self-diagnostic receiver circuit.

DETAILED DESCRIPTION OF THE INVENTION

Exemplary embodiments of the invention will be described with reference to the accompanying drawings. Like items in the drawings are shown with the same reference numbers.

Figure 2 shows a schematic of one embodiment of noise margin self-diagnostic receiver circuit. The receiver includes a data signal comparator 52 and a noise margin self-diagnostic circuit 50. The data comparator 52 receives a data

input 54 and generates an output 56 with respect to a predetermined reference voltage (VREF) for the signal. The self-diagnostic circuit 50 includes: two additional comparators 58, 60; two delay buffers 68a, 68b; four "flip-flop" circuits 62a - 62d; two "exclusive or"(XOR) logic gates 64a, 64b; a "not or" (NOR) logic gate; and a flag output 70.

In this embodiment, the data comparator 52 is a normal single ended data receiver. The comparator 52 itself may be a differential amplifier or a sense amplifier. The output of the comparator 52 is determined by whether the voltage of the data input signal 54 is higher or lower than the VREF. The comparison is made within an offset range. In some embodiments, the offset range may be ± 30mV. The other comparators 58, 60 function in the same manner, with the same physical characteristics as the data comparator with the exception of their reference voltage. The high comparator (COMP_H) 58 references the data input signal 54 to a pre-determined high voltage limit (VREF_H). Conversely, the low comparator (COMP_L) 60 references the data input signal 54 to a predetermined low voltage limit (VREF_L).

The output from each comparator feeds into the clock inputs of two separate flip-flop circuits 62a – 62d. Specifically in the embodiment shown, the output of COMP_H 58 feeds into the clock input of first flip-flop 62a and the clock input of the third flip-flop 62c. The output of COMP_H 58 first passes through a delay buffer 68b before being input into the third flip-flop 62c. The output of COMP_L 60 feeds into the clock input of second flip-flop 62b and the clock input of the fourth flip-flop 62d. The output of COMP_L 60 first passes through a delay buffer 68a before being input into the second flip-flop 62b. In

summary, the outputs of COMP_H 58 and COMP_L 60 provide the clock signal for the flip-flops 62a - 62d.

In this embodiment, each flip-flop 62a – 62d has an initial data bit value of "0". This is accomplished by use of a "power on reset" for each flip-flop 62a – 62d which automatically resets the data value to "0" when the circuit 50 is powered up. Upon receipt of a clock signal from COMP_H 58 or COMP_L 60, each flip-flop 62a – 62d will output a "1" to one of the XOR gates 64a, 64b. The output of these gates is then input into the NOR gate 66 and displayed as a flag on the alarm output 70. The value of the flag will then indicate if signal performance is normal or if a noise error has occurred.

As shown in Figure 1A, a normal signal with a digital LOW value will monotonously cross over VREF_L first, then VREF, and finally VREF_H before reaching a digital HIGH value. Conversely, a normal signal with a digital HIGH value with monotonously cross over VREF_H first, then VREF, and finally VREF_L before reaching a digital LOW value. In some embodiments of the present invention, the difference between the high voltage limit and the low voltage limit is 300 mV.

As shown in Figure 2, the circuit 50 may be broken down into two separate sections: a high-to-low section and a low-to-high section. Each section measures one of the transitions of the signal voltage and tests for errors in the transition. The high-to-low section includes the flip-flop 62a, the flip-flop 62b with delay buffer 68a and an XOR gate 64a. This section measures the transition of a signal voltage as it decreases in value through VREF_H, VREF, and VREF_L, respectively. The delay buffer 68a serves to delay the input from CMP_L 60 to

flip-flop 62b in order to prevent an error from too large a transition signal being received.

Conversely, the low-to-high section includes the flip-flop 62c, the flip-flop 62d with delay buffer 68b and an XOR gate 64b. This section measures the transition of a signal voltage as it increases in value through VREF_L, VREF, and VREF_H, respectively. The delay buffer 68b serves to delay the input from CMP_H 58 to flip-flop 62c in order to prevent an error from too large a transition signal being received.

During a signal transition, CMP_H 58 and CMP_L 60 will check the nature of the monotonous signal transition against the pre-set voltage boundaries of VREF_H and VREF_L, respectively. If the transition is normal as shown in Figure 1A, the decision logic of the circuit 50 will drive the value of the flag output to indicate a normal state at the alarm output 70. However, if the transition is in error due to voltage ring back, abnormal voltage levels, etc., the decision logic of the circuit 50 will drive the value of the flag output to indicate an error state at the alarm output 70.

The advantages of the disclosed invention includes the ability of a digital circuit to perform a self-diagnosis of signal noise error without pin-by-pin or other time intensive debugging methods. Another advantage of the disclosed invention includes the ability for the circuit to perform self-diagnosis of signal noise error in the test lab, at production quality control, or during actual usage.

While the invention has been disclosed with reference to specific examples of embodiments, numerous variations and modifications are possible. Therefore, it is intended that the invention not be limited by the description in the specification, but rather the claims that follow.